

IN THE CLAIMS

Please cancel claim 1 without prejudice or disclaimer.

Please amend claim 2 as indicated below.

This listing of claims will replace all prior versions, and listings, of the claims in the Application.

Listing of Claims:

1 1. (cancelled)

1 2. (currently amended) ~~The receiver as recited in claim 1,~~ A receiver
2 comprising:
3 an input configured to receive serial data;
4 an oscillator configured to generate phases of a clock; and
5 a retiming mechanism configured to receive said serial data and said phases of said
6 clock, wherein said retiming mechanism includes circuitry for reducing timing
7 uncertainties in said serial data by selecting a particular phase of said clock to be
8 asserted to sample said serial data during a period of said serial data, wherein each
9 particular phase of said clock to be asserted to sample said serial data during said
10 period of said serial data corresponds to a particular retiming state.

1 3. (previously presented) The receiver as recited in claim 2, wherein each
2 particular retiming state is paired with a particular synchronization state, wherein said
3 particular synchronization state indicates which particular phase of said clock to
4 assert at a given transition of said serial data.

1 4. (original) The receiver as recited in claim 3, wherein said retiming
2 mechanism comprises a first unit, wherein said first unit includes circuitry for
3 generating logical values of each particular synchronization state/retiming state pair.

1 5. (original) The receiver as recited in claim 4, wherein said first unit receives
2 said phases of said clock and said serial data.

1 6. (original) The receiver as recited in claim 5, wherein said first unit comprises
2 a sample clock mechanism configured to sample values of said phases of said clock.

1 7. (original) The receiver as recited in claim 6, wherein said first unit comprises
2 a plurality of second units, wherein said sampled phase values are inputted to said
3 plurality of second units, wherein said plurality of second units includes circuitry for
4 generating said logical values of each particular synchronization state/retiming state
5 pair.

1 8. (previously presented) The receiver as recited in claim 7, wherein said
2 plurality of second units outputs said logical values of each particular synchronization
3 state/retiming state pair to a completion detector, wherein said completion detector
4 includes circuitry for generating a signal indicating a time to sample inputs of said
5 completion detector.

1 9. (original) The receiver as recited in claim 8, wherein said first unit comprises
2 a third unit configured to detect one of said inputs of said completion detector that has
3 not changed state upon said completion detector generating said signal, wherein said
4 one of said inputs that did not change state corresponds to a particular
5 synchronization state/retiming state pair to be asserted.

1 10. (original) The receiver as recited in claim 7, wherein each of said plurality of
2 second units comprises circuitry for performing a NOR function on particular
3 sampled phase values.

1 11. (original) The receiver as recited in claim 8, wherein said completion detector
2 comprises circuitry for performing a NOR function on said logical values of each
3 particular synchronization state/retiming state pair outputted by said plurality of
4 second units.

1 12. (original) The receiver as recited in claim 1, wherein said oscillator operates
2 at a frequency lower than a data rate of said serial data.

1 13. (original) A system comprising:
2 a transmission medium;
3 a transmitter coupled to said transmission medium, wherein said transmitter is
4 configured to transmit data in a serial form; and
5 a receiver coupled to said transmission medium, wherein said receiver is
6 configured to receive said serial data, wherein said receiver comprises an oscillator
7 configured to generate phases of a clock, wherein said receiver further comprises a
8 retiming mechanism configured to receive said serial data and said phases of said
9 clock, wherein said retiming mechanism includes circuitry for reducing timing
10 uncertainties in said serial data by selecting a particular phase of said clock to be
11 asserted to sample said serial data during a period of said serial data.

1 14. (previously presented) The system as recited in claim 13, wherein each
2 particular phase of said clock to be asserted to sample said serial data during said
3 period of said serial data corresponds to a particular retiming state.

1 15. (previously presented) The system as recited in claim 14, wherein each
2 particular retiming state is paired with a particular synchronization state, wherein said
3 particular synchronization state indicates which particular phase of said clock to
4 assert at a given transition of said serial data.

1 16. (original) The system as recited in claim 15, wherein said retiming
2 mechanism comprises a first unit, wherein said first unit includes circuitry for
3 generating logical values of each particular synchronization state/retiming state pair.

1 17. (original) The system as recited in claim 16, wherein said first unit receives
2 said phases of said clock and said serial data.

1 18. (original) The system as recited in claim 17, wherein said first unit comprises
2 a sample clock mechanism configured to sample values of said phases of said clock.

1 19. (original) The system as recited in claim 18, wherein said first unit comprises
2 a plurality of second units, wherein said sampled phase values are inputted to said
3 plurality of second units, wherein said plurality of second units includes circuitry for
4 generating said logical values of each particular synchronization state/retiming state
5 pair.

1 20. (previously presented) The system as recited in claim 19, wherein said
2 plurality of second units outputs said logical values of each particular synchronization
3 state/retiming state pair to a completion detector, wherein said completion detector
4 includes circuitry for generating a signal indicating a time to sample inputs of said
5 completion detector.

1 21. (original) The system as recited in claim 20, wherein said first unit comprises
2 a third unit configured to detect one of said inputs of said completion detector that has

3 not changed state upon said completion detector generating said signal, wherein said
4 one of said inputs that did not change state corresponds to a particular
5 synchronization state/retiming state pair to be asserted.

1 22. (original) The system as recited in claim 19, wherein each of said plurality of
2 second units comprises circuitry for performing a NOR function on particular
3 sampled phase values.

1 23. (original) The system as recited in claim 20, wherein said completion detector
2 comprises circuitry for performing a NOR function on said logical values of each
3 particular synchronization state/retiming state pair outputted by said plurality of
4 second units.

1 24. (original) The system as recited in claim 13, wherein said oscillator operates
2 at a frequency lower than a data rate of said serial data.